

Seat No. : _____

NQ-114

November-2017

B.C.A., Sem.-III

CC-201 : Computer Organization and Advanced Microprocessors

Time : 3 Hours]

[Max. Marks : 70

- Instructions :** (1) Begin new answer on a new page.
(2) Draw diagrams wherever necessary.
(3) Figures to the right indicate full marks.

1. (A) Answer the following :

- (1) Explain Von Neumann Architecture with block diagram. **4**
(2) Write a note on interrupts and its types. **3**

OR

Answer the following :

- (1) Write a note on device controller. **4**
(2) Discuss macro and micro-operations. **3**

(B) Answer the following :

Explain instruction format with example. **7**

OR

Answer the following :

- (1) Write a note on bus with its usage. **4**
(2) Discuss CPU registers. **3**

2. (A) Answer the following :

Define Multiplexer. Explain 4 X 1 MUX with appropriate diagrams. **7**

OR

Answer the following :

Define Encoder. Write a note on Decimal-to-BCD Encoder.

(B) Answer the following :

- (1) Draw logic circuit and truth table of JK flip-flop. 4
- (2) Discuss normalization of floating point numbers with a suitable example. 3

OR

Answer the following :

- (1) Draw schematic diagram and truth table of full adder. 4
- (2) Describe IEEE representation of single precision floating point numbers. 3

3. (A) Answer the following :

- (1) Write a note on associative memory. 4
- (2) Discuss any two memory parameters. 3

OR

Answer the following :

- (1) Write a note on instruction prefetch.
- (2) Describe memory classification based on access methods.

(B) Answer the following :

What is mapping ? Write a note on direct mapping in cache memory. 7

OR

Answer the following :

Write a note on cache coherence with its solution.

4. (A) Answer the following :

Compare CISC and RISC processors. 7

OR

Answer the following :

Classify and explain various addressing modes of 8086.

(B) Answer the following :

- (1) Write a note on functional unit of 8086. 4
- (2) Discuss the features of Intel i7 processors. 3

OR

Answer the following :

- (1) Describe scalar and super scalar processors. 4
- (2) Write a note on Micro controllers. 3

- (1) _____ register stores the result of the last processing step of the ALU.
(a) Accumulator (AC)
(b) Instruction Register (IR)
(c) Memory Buffer Register (MBR)
(d) Memory Address Register (MAR)
- (2) The ratio of pulse width to time period is called _____.
(a) Clock frequency
(b) Clock cycle
(c) Duty cycle
(d) Clock pulse
- (3) A program that determines how a computer will communicate with a peripheral device is known as _____.
(a) System Manager
(b) Communication Manager
(c) Memory Controller
(d) I/O Controller
- (4) In IEEE representation of single precision floating point number, mantissa is of _____ bits.
(a) 32
(b) 23
(c) 52
(d) 64
- (5) When subtraction is performed in 2's complement system, if carry is generated, then it is _____.
(a) Added to minuend
(b) Dropped
(c) Subtracted from minuend
(d) None of the above
- (6) _____ bit is used to represent negative sign in signed magnitude form.
(a) -1
(b) -0
(c) 0
(d) 1
- (7) _____ is the access time taken by the first access in a series of accesses.
(a) Cycle time
(b) Frequency
(c) Latency
(d) Bandwidth
- (8) The performance of the cache is measured in terms of _____ ratio.
(a) Hit
(b) Miss
(c) Read
(d) Write
- (9) Cycle time (T_c) = _____ + Recovery Time (T_r)
(a) Access time (T_a)
(b) Turn around time (TA)
(c) Frequency (F)
(d) Latency time (Lt)
- (10) A _____ processor allows instruction level parallelism within a single processor.
(a) Vector
(b) Scalar
(c) Superscalar
(d) Array

- (11) In _____ addressing mode, operand is a part of the instruction.
(a) register (b) indexed
(c) direct (d) immediate
- (12) _____ address determines how far is the memory location from the starting address of the segment register.
(a) Status (b) Offset/Effective
(c) Instruction Pointer (d) Program Counter
- (13) _____ is two-state device which offers basic memory cell for sequential logic operations.
(a) Half adder (b) Multiplexer
(c) Encoder (d) Flip-flop
- (14) $1101.11 \times 1.11 =$ _____
(a) 111111.100 (b) 11000.0001
(c) 1101.1100 (d) 101010.111
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